MBM2764
M2764

■ MBM27C64-25, MBM27C64-30

CMOS 65,536-Bit UV Erasable and Electrically Programmable Read Only Memory

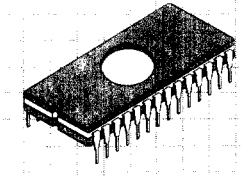
2764CCC

Description

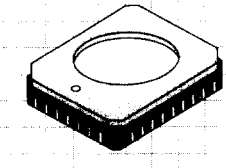
The Fujitsu MBM27C64 is a high speed 65,536-bit static Complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where the extremely low power consumption of CMOS is essential. The device dissipates only 40 mW/MHz when active, typically 5μW when in standby, yet it provides the same high speed performance as the NMOS MBM2764-type devices.

This package is available in either a Jedec Standard 28-pin dual-in-line package or a Jedec Standard 32-pin LCC package both of which have a transparent lid. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can be programmed into the memory.

The MBM27C64 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8192 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package DIP-28C-C01

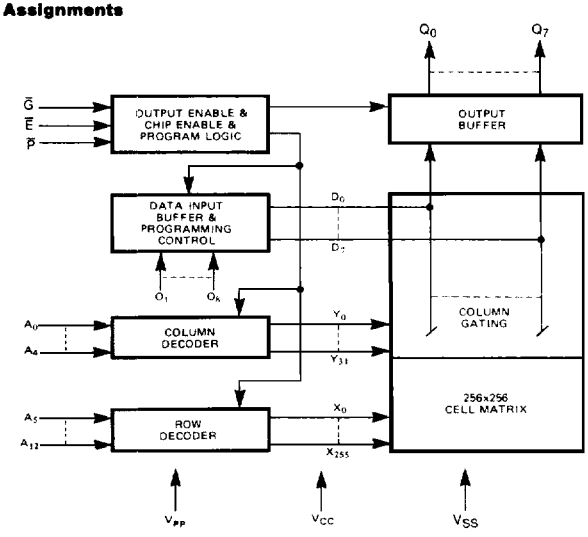


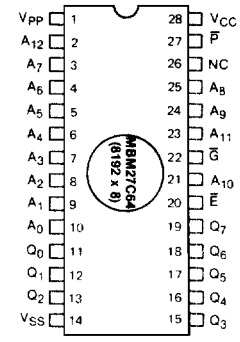
Leadless Chip Carrier LCC-32C-A01

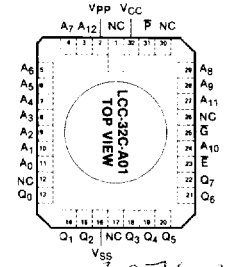
Features

- **CMOS Power Consumption:**
  550μW max. (Standby)
  5.5μW typ. (Standby)
  40mW/MHz (Active)
- **Fast Access Time:**
  MBM27C64-25 250 ns max.
  MBM27C64-30 300 ns max.
- **Utilizes the same simple programming requirements as MBM2764**
- **May be programmed 8 times faster than conventional methods using Fujitsu's QUICKPRO algorithm (see page 4-14)**
- **Single +5V operation**
- **10% V_{CC} tolerance standard**
- **TTL compatible inputs/outputs**
- **Three-state output provides OR-tie capability**
- **Output Enable $\overline{G}$ pin provides precise data bus control**
- **Pin and function compatible with 2764-type devices**
- **−40°C to +85°C and −55°C to +125°C temp. ranges available**

MBM27C64 Block Diagram and Pin Assignments







2764LCC

Absolute Maximum Ratings

(See Note)

Parameter	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to V_{SS}	V_{IN}, V_{OUT}	−0.6 to +7	V
V_{CC} with Respect to V_{SS}	V_{CC}	−0.6 to +7	V
V_{PP} with Respect to V_{SS}	V_{PP}	−0.6 to +22	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections

(V_{CC}(28) = +5, V_{SS}(14) = GND)

Mode	Function (DIP Pin No.) Address Input (2-10, 21, 23-25)	Data I/O (11-13, 15-19)	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	I_{CC} Supply (28)	V_{PP} (1)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC1}	V_{CC}
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH} / Don't Care	Don't Care / V_{IL}	I_{CC1}	V_{CC}
Stand By	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{SB1}	V_{CC}
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	I_{CC1}	V_{PP}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC1}	V_{PP}
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{SB1}	V_{PP}

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	8	12	pF

Recommended Operating Conditions
(Referenced to V_{SS} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage (Note 1)	V_{CC}	4.50	5.0	5.50	V	
Supply Voltage	V_{PP}	V_{CC} −0.6	—	V_{CC} +0.6	V	0°C to +70°C
Supply Voltage	V_{SS}	—	GND	—	V	Note 2
Input High Voltage	V_{IH}	2.0	—	V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.1	—	0.8	V	

Note 1. V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.
Note 2. −40°C to +85°C available as MBM27C64-25-X, MBM27C64-30-X −55°C to +125°C available as MBM27C64-30-W.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ (Note 1)	Max	Unit
Input Load Current (V_{IN} = 5.50V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.50V)	I_{LO}	—	—	10	μA
V_{PP} Supply Current	I_{PP}	—	1	100	μA
V_{CC} Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	—	—	1	mA
V_{CC} Standby Current ($\overline{E}$ = V_{CC} −0.3V to V_{CC} + 0.3V, I_{OUT} = 0mA)	I_{SB2}	—	1	100	μA
V_{CC} Active Current ($\overline{E}$ = V_{IL})	I_{CC1}	—	—	30	mA
V_{CC} Operation Current (f = 4MHz, I_{OUT} = 0mA)	I_{CC2}	—	—	30	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

Note 1. V_{CC} = 5.0V and TA = 25°C.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

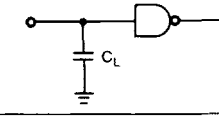
Parameter	Symbol	MBM27C64-25		MBM27C64-30		Unit
		Min	Max	Min	Max	
Address to Output Delay ($\overline{E}$ = $\overline{G}$ = V_{IL}, $\overline{P}$ = V_{IH})	TAVQV	—	250	—	300	ns
$\overline{E}$ to Output Delay ($\overline{G}$ = V_{IL}, $\overline{P}$ = V_{IH})	TELQV	—	250	—	300	ns
$\overline{G}$ to Output Delay ($\overline{E}$ = V_{IL}, $\overline{P}$ = V_{IH})	TGLQV	10	100	10	150	ns
$\overline{P}$ to Output Delay ($\overline{E}$ = $\overline{G}$ = V_{IL})	TPHQV	10	100	10	150	ns
Output Enable High to Output Float (See Note 2)	TGHQZ	0	60	0	105	ns
Address to Output Hold	TAXQX	0	—	0	—	ns

Note 2. TGHQZ is specified from $\overline{E}$, $\overline{G}$, or $\overline{P}$, whichever occurs first.

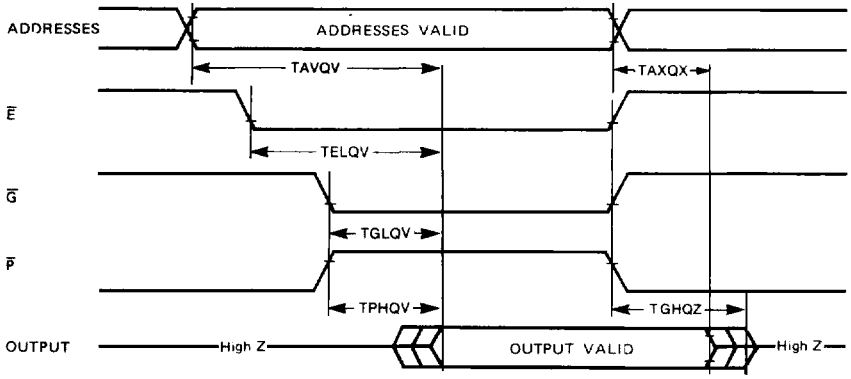
AC Test Conditions

Input Pulse Levels: 0.8 V to 2.2 V
Input Rise and Fall Time: ≤20nsec
Timing Measurement Reference Levels: 1.0 and 2.0V for inputs
0.8 and 2.0V for outputs
1 TTL gate and C_L = 100 pF

Output Load:



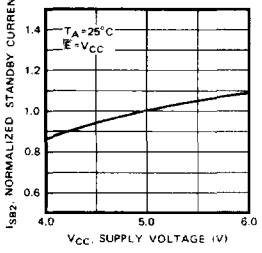
Operation Timing Diagram



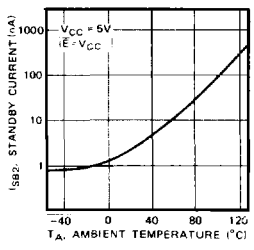
Note 3. $\overline{G}$ may be delayed up to TAVQV—TGLQV after the falling edge of $\overline{E}$ without impact on TAVQV.

Typical Characteristics Curves

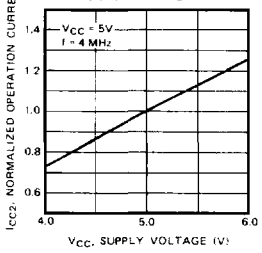
Standby Current vs Supply Voltage



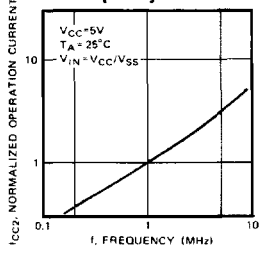
Standby Current vs Ambient Temperature



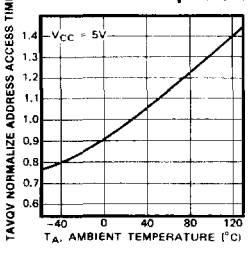
Operation Current vs Supply Voltage



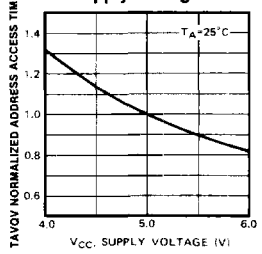
Operation Current vs Frequency



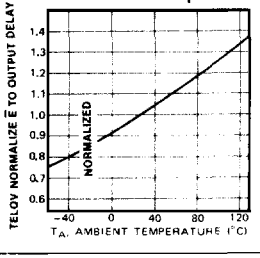
Address Access Time vs Ambient Temperature



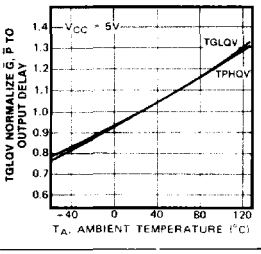
Address Access Time vs Supply Voltage



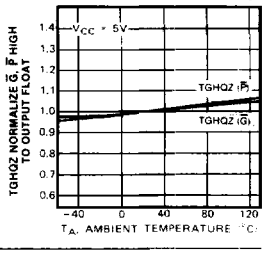
$\overline{E}$ to Output Delay vs Ambient Temperature



$\overline{G}$, $\overline{P}$ to Output Delay vs Ambient Temperature

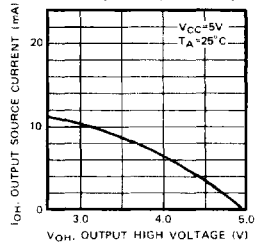


$\overline{G}$, $\overline{P}$ High to Output Float vs Ambient Temp

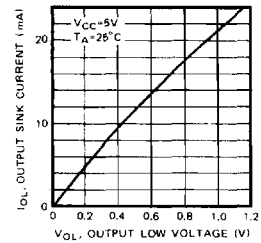


Typical Characteristics Curves, continued

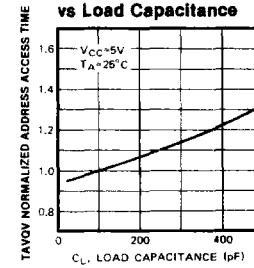
Output Source Current vs Output High Voltage



Output Sink Current vs Output Low Voltage



Address Access Time vs Load Capacitance



Programming/Erasing Information

Memory Cell Description

The MBM27C64 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C64 has all 65,536 bits in the "1" or high state. "0's" are loaded into the MBM27C64 through the procedure of programming.

Conventional Programming

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ and $\overline{P}$ are both at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. A pattern of eight bits are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the P input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{P}$ input is prohibited when programming.

Fig. 1 — Memory Cell

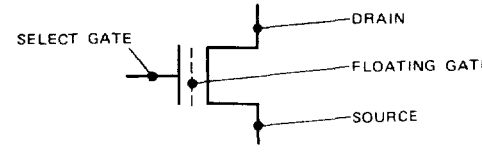
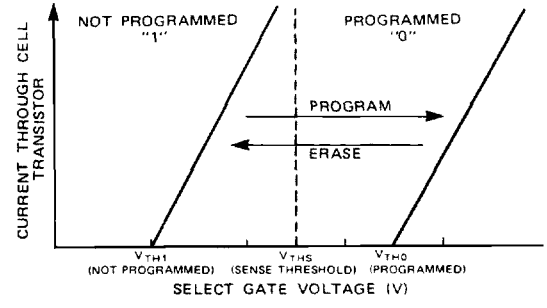


Fig. 2 — Memory Cell Threshold Shift



Programming/Erasing Information, continued

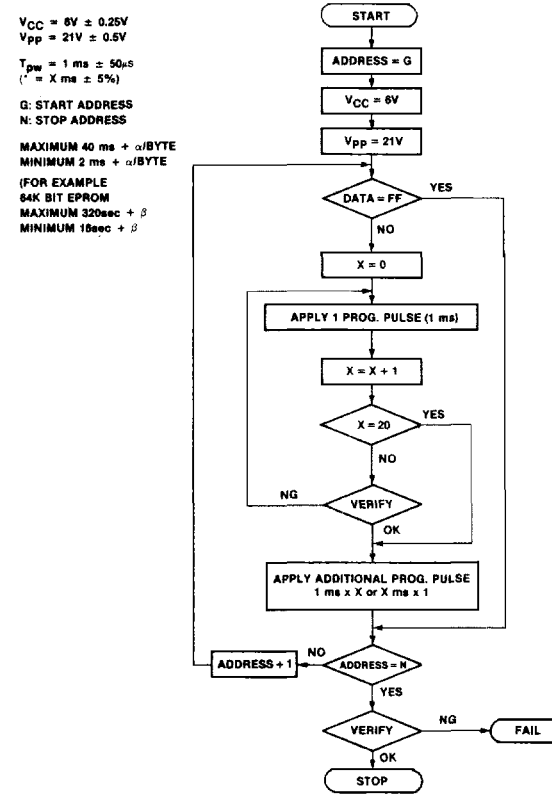
Quick Pro™ Programming
In addition to the standard 50 millisecond pulse width programming procedure, the MBM27C64 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulses to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the $\overline{E}$ input and a TTL high input must be applied to the $\overline{G}$ input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the $\overline{P}$ pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach proper stored charge levels.

Erasure
In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C64 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27C64. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2) for 15 to 20 minutes. The MBM27C64 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C64 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C64 and such exposure should be prevented to realize maximum data retention. If used in such an environment, the package windows should be covered by an opaque label or substance.

Fig. 3 — Quick Pro™ Program Flow Chart



QUICK PRO™ IS A TRADEMARK OF FUJITSU LIMITED

DC Characteristics

(T_A = 25 ±5°C,
V_{CC} = 5V ±10% (Conventional),
V_{CC} = 6V ± 0.25V (Quick Pro™)
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	10	μA	V_{IN} = 0.45V–5.25V
Output Low Voltage During Verify	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
Output High Voltage During Verify	V_{OH}	2.4	—	V	I_{OH} = −400mA
V_{CC} Supply Current	I_{CC1}	—	30	mA	—
Input Low Voltage	V_{IL}	−0.1	0.8	V	—
Input High Voltage	V_{IH}	2.0	V_{CC} +0.3	V	—
V_{PP} Supply Current During Programming Pulse	I_{PP2}	—	30	mA	E = P = V_{IL}

Note 1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

Note 2. V_{PP} must not be greater than 21.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{E}$ = $\overline{P}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 21 volts or vise-versa.

AC Characteristics

(T_A = 25 ±5°C,
V_{CC} = 5V ±10% (Conventional),
V_{CC} = 6V ± 0.25V (Quick Pro™)
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	TAVPL	2	—	—	μs
$\overline{E}$ Setup Time	TELPL	2	—	—	μs
Data Setup Time	TDVPL	2	—	—	μs
Address Hold Time	TGHAX	0	—	—	μs
Data Hold Time [1]	TPHDZ	2	—	—	μs
Chip Enable to Output Float Delay	TGHQZ	0	—	130	ns
V_{PP} Setup Time	TVPPHPL	2	—	—	μs
$\overline{P}$ Pulse Width-Conventional	TPLPH	25	50	55	ms
$\overline{P}$ Pulse Width-Quick-Pro™	TPLPH	0.95	1.00	1.05	ms
$\overline{G}$ Setup Time [1]	TDZGL	2	—	—	μs
Data Valid from $\overline{G}$	TGLQV	—	—	150	ns

Note [1] TPHDZ + TDZGL ≥ 50μs.

Programming Waveform