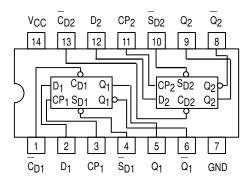
DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

The MC54/74F74 is a \underline{d} ual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, Q) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

• ESD > 4000 Volts

CONNECTION DIAGRAM



FUNCTION TABLE (Each Half)

Input	Outputs				
@ t _n	@ t _n + 1				
D	Q Q				
L	L H				
Н	H L				

Asynchronous Inputs:

LOW Input to \overline{S}_D sets Q to HIGH level

LOW Input to \overline{C}_D sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on \overline{C}_D and \overline{S}_D makes both Q and \overline{Q} HIGH

H = HIGH Voltage Level L = LOW Voltage Level

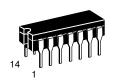
t_n = Bit time before clock pulse

 $t_n + 1$ = Bit time after clock pulse

MC54/74F74

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

FAST™ SCHOTTKY TTL



J SUFFIX CERAMIC CASE 632-08



N SUFFIX PLASTIC CASE 646-06

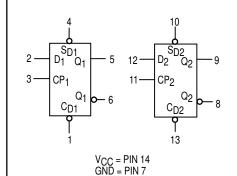


D SUFFIX SOIC CASE 751A-02

ORDERING INFORMATION

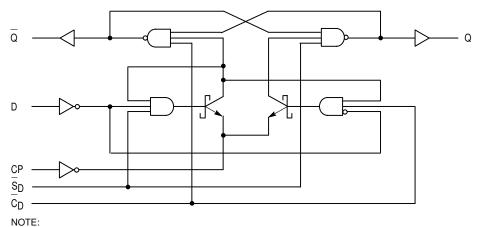
MC54FXXJ Ceramic MC74FXXN Plastic MC74FXXD SOIC

LOGIC SYMBOL



AST ORDER 31/03/99

LOGIC DIAGRAM



This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

ı	Symbol	Parameter		Min	Тур	Max	Unit
	V _C C	Supply Voltage	54, 74	4.50	5.0	5.50	V
	TA	Operating Ambient Temperature Range	54	- 55	25	125	°C
			74	0	25	70	
	lOH	Output Current — High	54, 74			-1.0	mA
	loL	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

DC CHARA	ACTERISTICS OVER OPERA	(unless o	rierwise specified)					
			Limits					
Symbol	Parameter		Min	Тур	Max	Unit	Test Conditions	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
	54 7		2.5	3.4		V	I _{OH} = -1.0 mA	V _{CC} = 4.50 V
VOH	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20mA	V _{CC} = MIN
lн	Input HIGH Current	nput HIGH Current			20	μΑ	V _{IN} = 2.7 V	V _{CC} = MAX
					100	μΑ	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current (CP and D Inputs)				-0.6	mA	V _{IN} = 0.5V	V _{CC} = MAX
	(C _D and S _D Inputs)				-1.8	mA		
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
Icc	Power Supply Current			10.5	16	mA	VCP = 0 V	V _{CC} = MAX

NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more then one output should be shorted at a time, nor for more than 1 second.

MC54/74F74

AC CHARACTERISTICS

		54/	74F	5	4F	74F			1
		T _A = +25°C		T _A = -55°C to +125°C		T _A = 0°C to 70°C			ı
		V _{CC} = +5.0 V		V_{CC} = 5.0 V \pm 10%		$V_{CC} = 5.0 \text{ V} \pm 10\%$			ı
		C _L = 50 pF		C _L = 50 pF		C _L = 50 pF			ı
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit	
f _{max}	Maximum Clock Frequency	100		100		100		MHz]
^t PLH	Propagation Delay	3.8	6.8	3.8	8.5	3.8	7.8	no	1
^t PHL	CP _n to Q _n or Q _n	4.4	8.0	4.4	10.5	4.4	9.2	ns	
^t PLH	Propagation Delay	2.5	6.1	2.5	8.0	2.5	7.1	no	1
tPHL	C_{Dn} or S_{Dn} to Q_n or Q_n	3.5	9.0	3.5	11.5	3.5	10.5	ns	

AC OPERATING REQUIREMENTS

		54/74F		54F		74F			
		T _A = +25°C		T _A = -55°C to +125°C		T _A = 0°C to +70°C			
		l v	V _{CC} = +5.0 V		V _{CC} = 5.0 V ± 10%		V _{CC} = 5.0V ± 10%		
Symbol	Parameter	Min	Тур	Max	Min	Max	Min	Max	Unit
t _S (H)	Setup Time, HIGH or LOW	2.0			3.0		2.0		
t _S (L)	D _n to CP _n	3.0			4.0		3.0		
t _h (H)	Hold Time, HIGH or LOW	1.0			2.0		1.0		ns
t _h (L)	D _n to CP _n	1.0			2.0		1.0		
t _W (H)	CP _n Pulse Width, HIGH	4.0			4.0		4.0		
t _w (L)	or LOW	5.0			6.0		5.0		ns
t _W (L)	C _{Dn} or S _{Dn} Pulse Width, LOW	4.0			4.0		4.0		ns
t _{rec}	Recovery Time C _{Dn} or S _{Dn} to CP	2.0			3.0		2.0		ns

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